19-3046; Rev 2; 6/04

EVALUATION KIT AVAILABLE

Two-Switch Power ICs with Integrated Power MOSFETs and Hot-Swap Controller

General Description

The MAX5042/MAX5043 isolated multimode PWM power ICs feature integrated switching power MOSFETs connected in a voltage-clamped, two-transistor, power-circuit configuration. These devices operate from a wide 20V to 76V input voltage range. The MAX5042 includes a hot-swap controller for use with an external power MOSFET to limit inrush current for applications where the power supply is plugged into a live power backplane. The MAX5043 does not include a hot-swap controller.

The voltage-clamped power topology of the MAX5042/MAX5043 enables full recovery of stored magnetizing and leakage inductive energy for enhanced efficiency and reliability. Operating at up to 500kHz switching frequency, these devices provide up to 50W of output power. The MAX5042/MAX5043 allow the implementation of both forward and flyback voltage or current-mode converter topologies. A dedicated latched external shutdown provides protection in addition to internal thermal shutdown.

The MAX5042/MAX5043 achieve higher efficiency when used with secondary-side synchronous rectification. These devices generate a look-ahead signal for driving secondary-side synchronous rectifiers.

The MAX5042/MAX5043 are rated for operation over the -40°C to +125°C and -40°C to +85°C temperature range, respectively, and are available in a small surface-mount 56-pin thin QFN package.

Warning: The MAX5042/MAX5043 are designed to work with high voltages. Exercise caution.

Applications

High-Efficiency Telecom/Datacom Power Supplies

Router/Switch Cards with 48V Backplane Power Systems

Servers with 48V Backplane Power Systems

xDSL Line Cards

xDSL Line-Driver Power Supplies

Distributed Power Systems with 48V Bus

42V Automotive Power Supplies

Power-Supply Modules

Pin Configurations appear at end of data sheet.

Features

- ♦ **Reliable Single-Stage Clamped Two-Switch Power ICs for High Efficiency**
- ♦ **No Reset Winding Required**
- ♦ **Up to 50W Output Power**
- ♦ **Integrated High-Voltage 75mΩ Power MOSFETs**
- ♦ **20V to 76V Wide Input Voltage Range**
- ♦ **Feed-Forward Voltage or Current-Mode Control**
- ♦ **Programmable Brownout Undervoltage Lockout**
- ♦ **Integrated Current Signal Amplifier for High-Efficiency, Current-Mode Control**
- ♦ **Internal Overtemperature Shutdown**
- ♦ **Indefinite Short-Circuit Protection**
- ♦ **Integrated Thermally Protected High-Voltage Startup Linear Regulator**
- ♦ **Integrated Hot-Swap Controller (MAX5042)**
- ♦ **Integrated Look-Ahead Signal Output Drives High-Speed Optocoupler for Secondary-Side Synchronous Rectification**
- ♦ **>90% Efficiency with Synchronous Rectification**
- ♦ **Up to 500kHz Switching Frequency**
- ♦ **High-Power, Small-Footprint 56-Pin Thermally Enhanced QFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5042ATN	-40°C to +125°C	56 Thin QFN
MAX5043ETN	-40°C to +85°C	56 Thin QFN

Selector Guide

PART	DESCRIPTION
MAX5042	Two-Switch Power IC with Integrated Power MOSFETs and Hot-Swap Controller for Isolated Power Supplies
MAX5043	Two-Switch Power IC with Integrated Power MOSFETs for Isolated Power Supplies

Two-Switch Power ICs with Integrated Power MOSFETs and Hot-Swap Controller

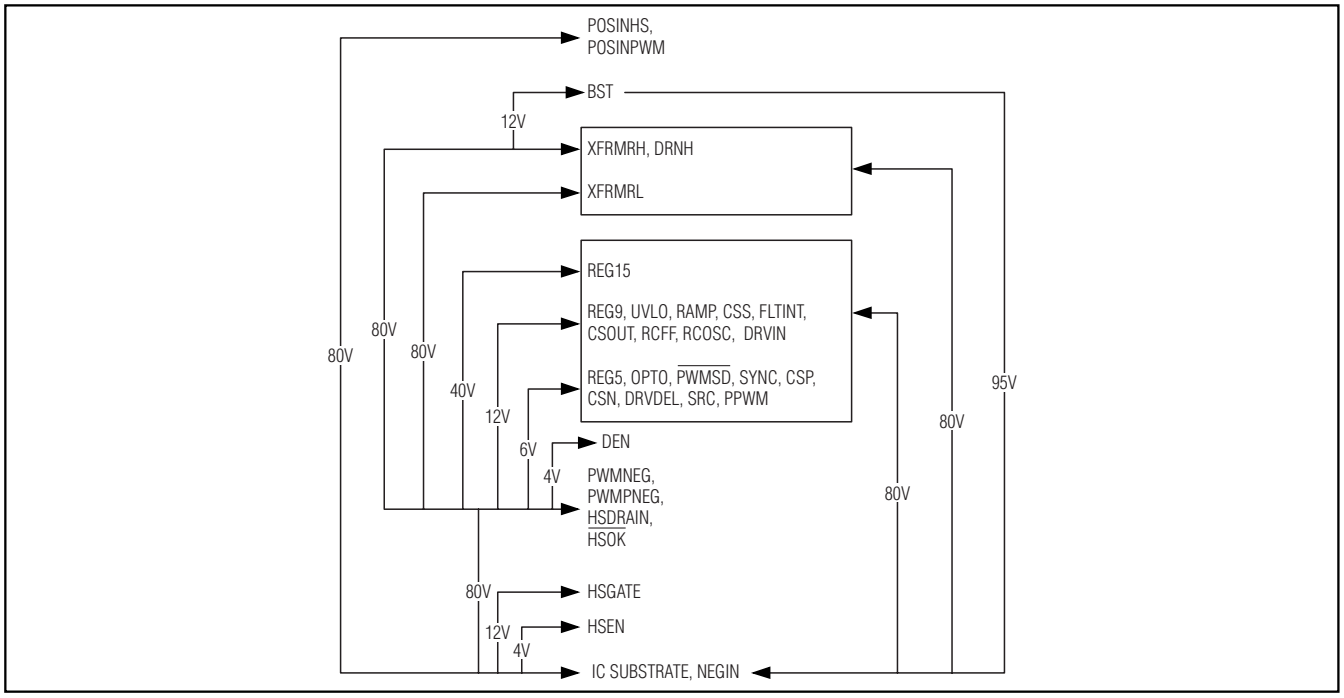
ABSOLUTE MAXIMUM RATINGS

(See the *Absolute Maximum Ratings Diagram* below to better understand the absolute maximum ratings of the various blocks.)

PWMNEG, POSINPWM, DRNH, XFRMRH, XFRMRL, SRC to NEGIN .....-0.3V to +80V
BST to NEGIN .....-0.3V to +95V
BST to XFRMRH .....-0.3V to +12V
SRC to PWMNEG .....-0.3V to +6V
REG15 to PWMNEG .....-0.3V to +40V
REG15 to POSINPWM .....-80V to +0.3V
REG9, DRVIN to PWMNEG .....-0.3V to +12V
REG5 to PWMNEG .....-0.3V to +6V
REG15 Current .....±80mA
REG9 Current 40mA
REG5 Current 20mA
UVLO, RAMP, CSS, FLTINT, CSOUT, RCFF, RCOSC to PWMNEG .....-0.3V to +12V
OPTO, PWMSD, SYNC, CSP, CSN, DRVDEL to PWMNEG .....-0.3V to +6V
PPWM to PWMNEG .....-0.3V to (REG5 + 0.3V)
PPWM Current .....±20mA
PWMPNEG to PWMNEG .....-0.3V to +0.3V
DRNH Continuous Average Current (all pins combined)
T_J = +125°C 2A
T_J = +150°C 1.4A
XFRMRH Continuous Average Current (all pins combined)
T_J = +125°C 2A
T_J = +150°C 1.4A
XFRMRL Continuous Average Current (all pins combined)
T_J = +125°C 2A
T_J = +150°C 1.4A
SRC Continuous Current (all pins combined)
T_J = +125°C 2A
T_J = +150°C 1.4A
POSINHS to NEGIN .....-0.3V to +80V
HSEN to NEGIN .....-0.3V to +4V
DEN to PWMNEG .....-0.3V to +4V
HSGATE to NEGIN .....-0.3V to +12V
HSDRAIN, HSOK to NEGIN .....-0.3V to +80V
HSOK Current 20mA
Continuous Power Dissipation (T_A = +70°C)
56-Pin Thin QFN (derate 47.6mW/°C above +70°C) 3.8W
Junction to Ambient Thermal Resistance, θ_{JA} .....+21°C/W
Operating Temperature Range
MAX5042ATN .....-40°C to +125°C
MAX5043ETN .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute Maximum Ratings Diagram



ELECTRICAL CHARACTERISTICS

($V_{POSINPWM}$ = 20V to 76V, V_{REG15} = 18V, C_{REG15} = 4.7µF, C_{REG9} = 1µF, C_{REG5} = 1µF, R_{RCOSC} = 24kΩ, C_{RCOSC} = 100pF, C_{BST} = 0.22µF, R_{DRVDEL} = 10kΩ, C_{DRVDEL} = 0.22µF, V_{CSS} = V_{CSP} = V_{CSN} = V_{RAMP} = V_{PWMNEG} = V_{NEGIN} = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at $V_{POSINPWM}$ = 48V, T_A = +25°C, unless otherwise noted. All voltages are referred to PWMNEG, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Range	$V_{POSINPWM}$		20		76	V
REG15 REGULATOR						
REG15 Output Voltage Range	V_{REG15}	$V_{POSINPWM}$ = 20V to 76V	13.0		16.6	V
REG15 Output Voltage Load Regulation		$V_{POSINPWM}$ = 20V, I_{REG15} = 0 to 80mA			1.5	V
REG15 Output Current		Inferred from load regulation test			80	mA
REG15 Current Limit		REG15 shorted to PWMNEG with 10Ω		140		mA
REG15 Overdrive Voltage			18		40	V
REG9 REGULATOR						
REG9 Output Voltage Range		V_{REG15} = 18V to 40V	8.3		10.1	V
REG9 Output Voltage Load Regulation		I_{REG9} = 0 to 40mA			0.35	V
REG9 Output Current		Inferred from load regulation test			40	mA
REG9 Current Limit		REG9 shorted to PWMNEG with 10Ω		100		mA
REG5 REGULATOR						
REG5 Output Voltage Range		V_{REG15} = 18V to 40V	4.5		5.5	V
REG5 Output Voltage Load Regulation		I_{REG5} = 0 to 20mA			0.35	V
REG5 Output Current		Inferred from load regulation test			20	mA
REG5 Current Limit		REG5 shorted to PWMNEG with 10Ω		40		mA
PWM COMPARATOR						
Common-Mode Range	V_{CM-PWM}		0		5.5	V
Input Offset Voltage				10		mV
Input Bias Current			-2.5		+2.5	µA
Propagation Delay		50mV overdrive, 0 ≤ V_{CM-PWM} ≤ 5.5V		70		ns
RCOSC OSCILLATOR						
PWM Period	$t_{OSC-PWM}$			3.9		µs
Maximum Duty Cycle				47		%
Maximum RCOSC Frequency	f_{RCOSC}			1.2		MHz
RCOSC Peak Trip Level	V_{TH}			2.55		V
RCOSC Valley Trip Level				0.2		V
RCOSC Input Bias Current				-0.3		µA
RCOSC Discharge MOSFET $R_{DS(ON)}$		Sinking 10mA		60	120	Ω
RCOSC Discharge Pulse Width				50		ns
SYNC High Level			3.5			V
SYNC Low Level					0.8	V

ELECTRICAL CHARACTERISTICS (continued)

($V_{POSINPWM}$ = 20V to 76V, V_{REG15} = 18V, C_{REG15} = 4.7µF, C_{REG9} = 1µF, C_{REG5} = 1µF, R_{RCOSC} = 24kΩ, C_{RCOSC} = 100pF, C_{BST} = 0.22µF, R_{DRVDEL} = 10kΩ, C_{DRVDEL} = 0.22µF, V_{CSS} = V_{CSP} = V_{CSN} = V_{RAMP} = V_{PWMNEG} = V_{NEGIN} = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at $V_{POSINPWM}$ = 48V, T_A = +25°C, unless otherwise noted. All voltages are referred to PWMNEG, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNC Leakage Current					±1	µA
SYNC Maximum Frequency	f_{SYNC}			2.4		MHz
SYNC On-Time			50			ns
SYNC Off-Time			200			ns
PWM LOGIC						
PWM Comparator Propagation Delay				70		ns
PPWM to XFRMRL Delay		PPWM rising		120		ns
DRVDEL Reference Voltage			1.14		1.38	V
PPWM Output High		Sourcing 2mA	2.8			V
PPWM Output Low		Sinking 2mA			0.4	V
$\overline{PWMSD}$ Logic High			3.5			V
$\overline{PWMSD}$ Logic Low					0.8	V
$\overline{PWMSD}$ Leakage Current					±1	µA
SOFT-START						
Soft-Start Current	I_{CSS}			33		µA
Minimum OPTO Voltage		CSS = 0, sinking 2mA		1.4		V
RAMP GENERATOR						
Minimum RCFF Voltage		RCFF sinking 2mA		2.1		V
RCFF Leakage				±0.1	±1	µA
OVERLOAD FAULT						
FLTINT Pulse Current	I_{FLTINT}			80		µA
FLTINT Trip Point			2.0	2.7	3.5	V
FLTINT Hysteresis				0.75		V
INTERNAL POWER FETs						
On-Resistance	R_{DSON}	V_{DRVIN} = V_{BST} = 9V, V_{XFRMRH} = V_{SRC} = 0, I_{DS} = 190mA		75	200	mΩ
Off-State Leakage Current					10	µA
Total Gate Charge Per FET		Inferred from supply current with V_{DS} = 50V		45		nC
HIGH-SIDE DRIVER						
Low-to-High Latency		Driver delay until FET V_{GS} reaches 0.9 x (V_{BST} - V_{XFRMRH})		80		ns
High-to-Low Latency		Driver delay until FET V_{GS} reaches 0.1 x (V_{BST} - V_{XFRMRH})		45		ns
Output Drive Voltage		BST to XFRMRH with high side on		8		V
LOW-SIDE DRIVER						
Low-to-High Latency		Driver delay until FET V_{GS} reaches 0.9 x V_{DRVIN}		80		ns

ELECTRICAL CHARACTERISTICS (continued)

($V_{POSINPWM}$ = 20V to 76V, V_{REG15} = 18V, C_{REG15} = 4.7µF, C_{REG9} = 1µF, C_{REG5} = 1µF, R_{RCOSC} = 24kΩ, C_{RCOSC} = 100pF, C_{BST} = 0.22µF, R_{DRVDEL} = 10kΩ, C_{DRVDEL} = 0.22µF, V_{CSS} = V_{CSP} = V_{CSN} = V_{RAMP} = V_{PWMNEG} = V_{NEGIN} = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at $V_{POSINPWM}$ = 48V, T_A = +25°C, unless otherwise noted. All voltages are referred to PWMNEG, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High-to-Low Latency		Driver delay until FET V_{GS} reaches 0.1 x V_{DRVIN}		45		ns
CURRENT-SENSE COMPARATOR						
Current-Limit-Comparator Threshold Voltage			140	156	172	mV
Current-Limit-Comparator Propagation Delay		10mV overdrive		40		ns
CURRENT-SENSE AMPLIFIER						
Current Amplifier Gain		V_{CSN} = 0, V_{CSP} = 0 to 0.35V	9.75	10	10.25	V/V
Input Voltage Offset		V_{CN} = V_{CSP} = -0.3V to +0.3V	185	200	230	mV
Input Common-Mode Range			-0.3		+0.3	V
Input Differential-Mode Range		Inferred from current amplifier gain test			0.35	V
CSP Input Bias Current		V_{CSP} = -0.3V to +0.3V, V_{CSN} = 0	-160		-40	µA
CSN Input Bias Current		V_{CSP} = -0.3V to +0.3V, V_{CSN} = 0	-160		-30	µA
Settling Time		V_{CSN} = 0, V_{CSP} steps from 0 to 0.2V, 10% settling time, C_L = 20pF		70		ns
3dB Bandwidth				7		MHz
BOOST VOLTAGE CIRCUIT						
QB $R_{DS(ON)}$		Sinking 100mA		10	20	Ω
Driver Output Delay				200		ns
One-Shot Pulse Width				300		ns
THERMAL SHUTDOWN						
Shutdown Temperature		Temperature rising		150		°C
Thermal Hysteresis				14.5		°C
PWM CONVERTER UNDERVOLTAGE LOCKOUT (UVLO)						
Preset UVLO Threshold		Measured at POSINPWM rising	28	31	34	V
UVLO Threshold Hysteresis				3		V
UVLO Resistance		Looking into UVLO	30		75	kΩ
UVLO Trip Point		Measured at UVLO rising	1.15	1.27	1.39	V
UVLO Hysteresis				+127		mV
Preset DEN Threshold		MAX5043 only, measured at POSINPWM rising	27		34	V
DEN Threshold Hysteresis		MAX5043 only		3.1		V
DEN Startup Delay		MAX5043 only	3.5	12	27.0	ms
DEN Turn-Off Delay		MAX5043 only	0.2	0.7	1.5	ms
DEN Trip Point		MAX5043 only, rising with respect to PWMNEG	1.11		1.35	V

ELECTRICAL CHARACTERISTICS (continued)

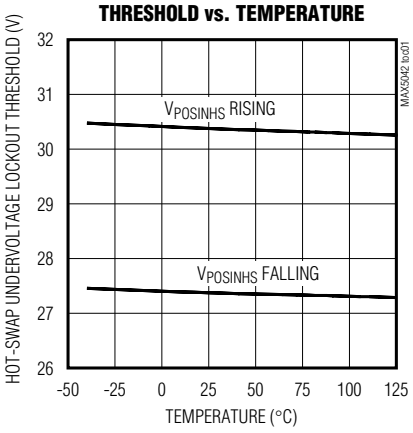
($V_{POSINPWM}$ = 20V to 76V, V_{REG15} = 18V, C_{REG15} = 4.7µF, C_{REG9} = 1µF, C_{REG5} = 1µF, R_{RCOSC} = 24kΩ, C_{RCOSC} = 100pF, C_{BST} = 0.22µF, R_{DRVDEL} = 10kΩ, C_{DRVDEL} = 0.22µF, V_{CSS} = V_{CSP} = V_{CSN} = V_{RAMP} = V_{PWMNEG} = V_{NEGIN} = 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at $V_{POSINPWM}$ = 48V, T_A = +25°C, unless otherwise noted. All voltages are referred to PWMNEG, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DEN Hysteresis		MAX5043 only		124		mV
DEN Input Resistance		MAX5043 only, looking into DEN	18		55	kΩ
SUPPLY CURRENT						
Supply Current		From $V_{POSINHS}$ = $V_{POSINPWM}$ = 76V, CSS shorted to PWMNEG, REG15 = 18V		2	3	mA
		From REG15 = 18V, $V_{POSINHS}$ = $V_{POSINPWM}$ = 76V, CSS shorted to PWMNEG		6	8.5	
		From REG15 = 18V, $V_{POSINHS}$ = $V_{POSINPWM}$ = 76V, V_{DRNH} = V_{XFRMRH} = V_{XFRMRL} = V_{SRC} = 0V		20		
Standby Supply Current		MAX5042 only, $V_{POSINHS}$ = $V_{POSINPWM}$ = V_{PWMNEG} = $V_{PWMPNEG}$ = $V_{HSDRAIN}$ = 76V, HSEN = NEGIN		0.6	1	mA
HOT-SWAP CONTROLLER (MAX5042 Only)						
Hot-Swap UVLO Threshold		POSINHS with respect to NEGIN, voltage rising	27		34	V
Hot-Swap UVLO Hysteresis				3.1		V
Hot-Swap UVLO Resistance		Looking into HSEN	18		55	kΩ
Startup Delay		From HSEN rising to $\overline{HSOK}$ falling	50	165	350	ms
HSEN Turn-Off Delay		From HSEN falling to $\overline{HSOK}$ rising	3	10	25	ms
$\overline{HSOK}$ Output-High Leakage Current					±1	µA
HSEN Reference Threshold		Rising with respect to NEGIN	1.11		1.35	V
HSEN Hysteresis				124		mV
$\overline{HSOK}$ Output Low Voltage		Sinking 5mA			0.4	V
HSGATE Voltage High			7.5		10.0	V
Hot-Swap Slew Rate		C_L = 10µF, from HSDRAIN to NEGIN		10		V/ms

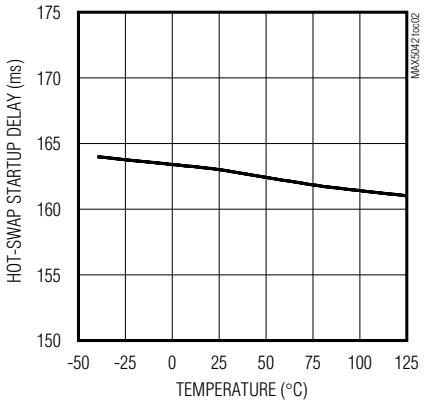
Typical Operating Characteristics

($V_{POSINPWM}$ = 20V, T_A = +25°C, unless otherwise noted.)

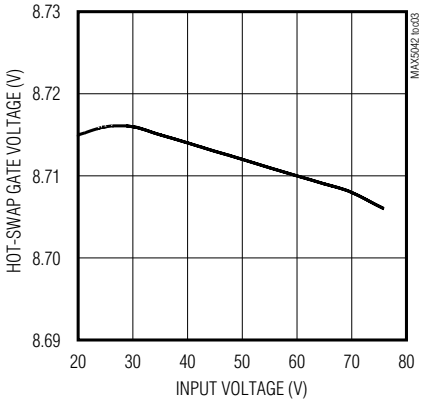
HOT-SWAP UNDERVOLTAGE LOCKOUT THRESHOLD vs. TEMPERATURE



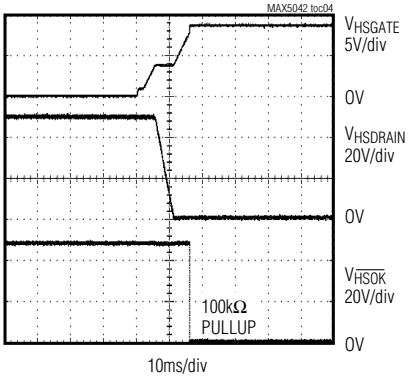
HOT-SWAP STARTUP DELAY vs. TEMPERATURE



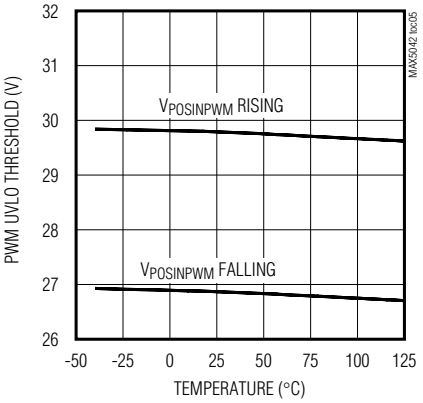
HOT-SWAP GATE VOLTAGE vs. INPUT VOLTAGE



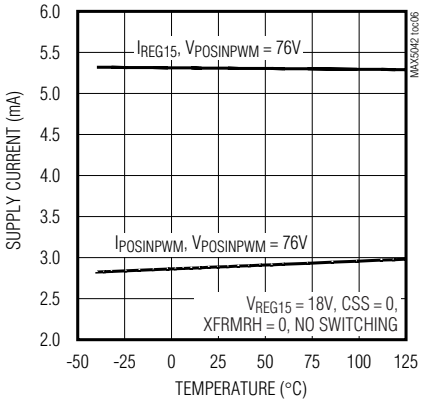
HOT-SWAP STARTUP WAVEFORM



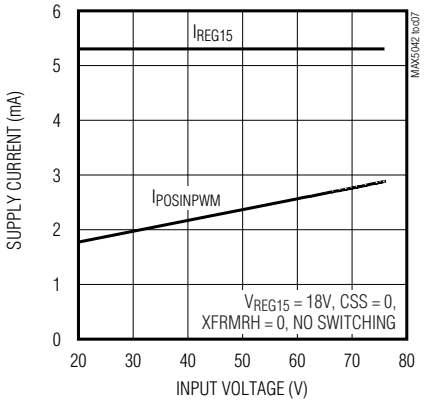
PWM UNDERVOLTAGE LOCKOUT THRESHOLD vs. TEMPERATURE



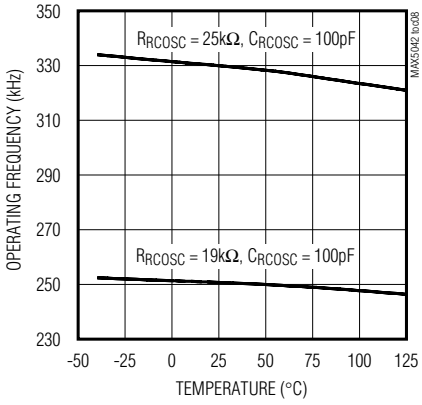
POSINPWM INPUT CURRENT, REG15 INPUT CURRENT vs. TEMPERATURE



POSINPWM INPUT CURRENT, REG15 INPUT CURRENT vs. INPUT VOLTAGE



OPERATING FREQUENCY vs. TEMPERATURE

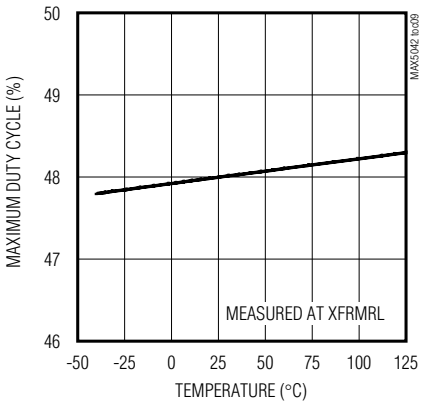


Two-Switch Power ICs with Integrated Power MOSFETs and Hot-Swap Controller

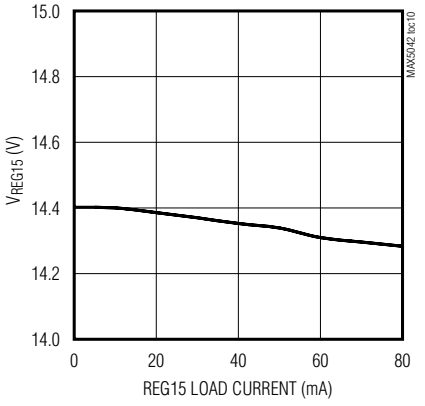
Typical Operating Characteristics (continued)

($V_{POSINPWM}$ = 20V, T_A = +25°C, unless otherwise noted.)

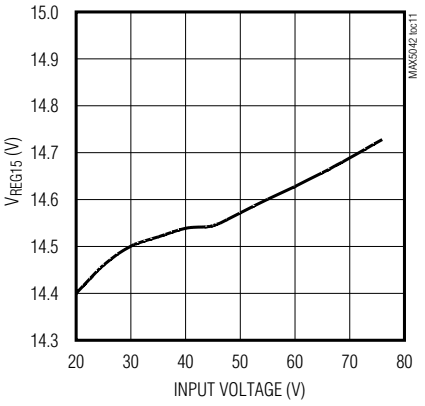
MAXIMUM DUTY CYCLE vs. TEMPERATURE



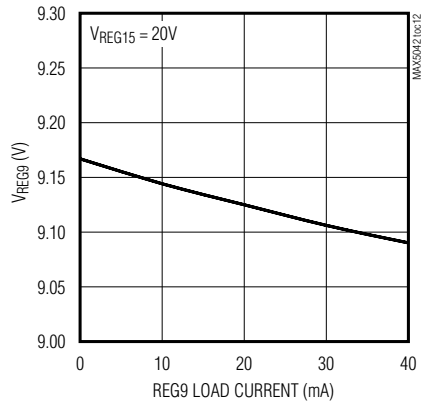
REG15 VOLTAGE vs. REG15 LOAD CURRENT



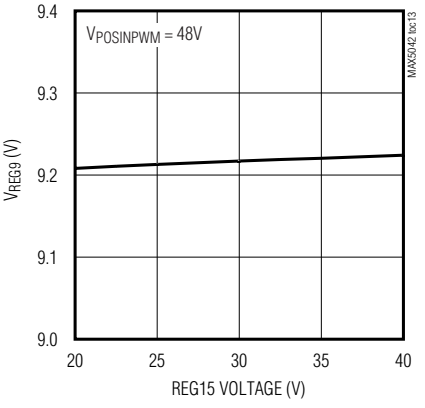
REG15 VOLTAGE vs. INPUT VOLTAGE



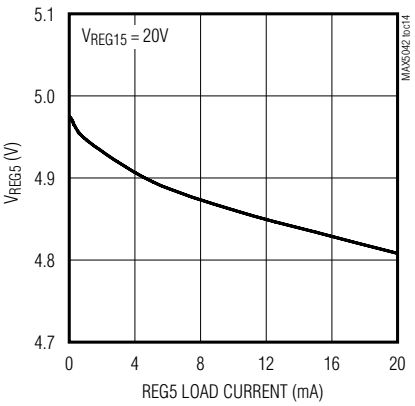
REG9 VOLTAGE vs. REG9 LOAD CURRENT



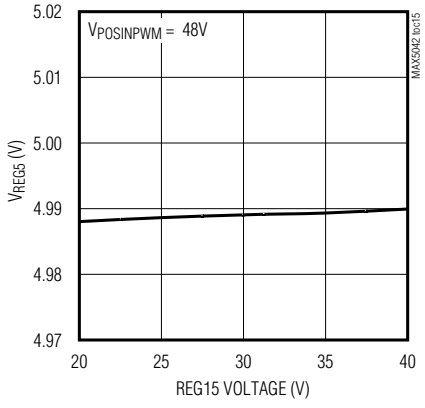
REG9 OUTPUT VOLTAGE vs. REG15 VOLTAGE



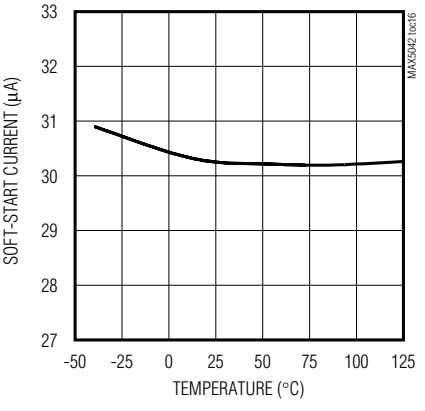
REG5 VOLTAGE vs. REG5 LOAD CURRENT



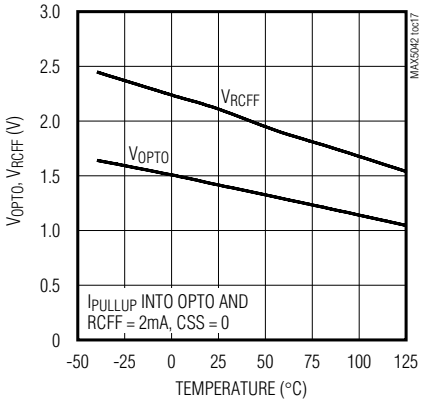
REG5 OUTPUT VOLTAGE vs. REG15 VOLTAGE



SOFT-START CURRENT vs. TEMPERATURE



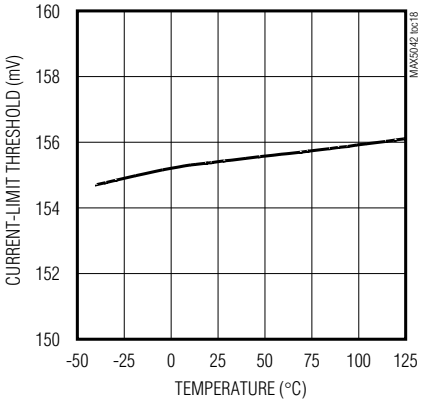
MINIMUM RCFF LEVEL, MINIMUM OPTO LEVEL vs. TEMPERATURE



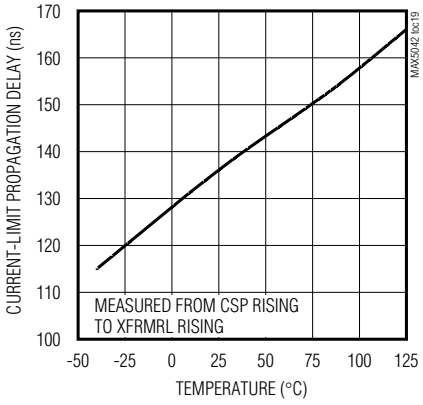
Typical Operating Characteristics (continued)

($V_{POSINPWM}$ = 20V, T_A = +25°C, unless otherwise noted.)

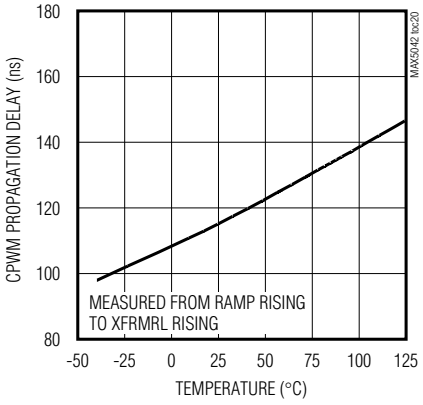
CURRENT-LIMIT THRESHOLD vs. TEMPERATURE



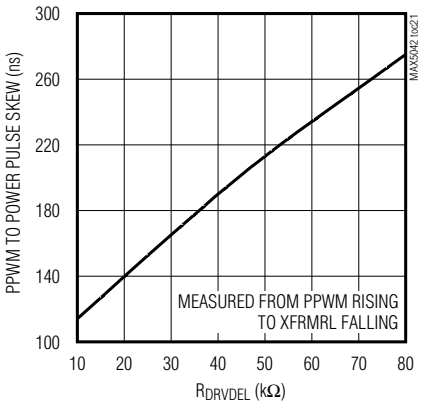
CURRENT-LIMIT PROPAGATION DELAY vs. TEMPERATURE



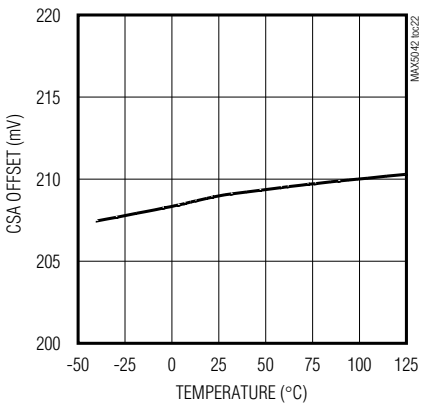
CPWM PROPAGATION DELAY vs. TEMPERATURE



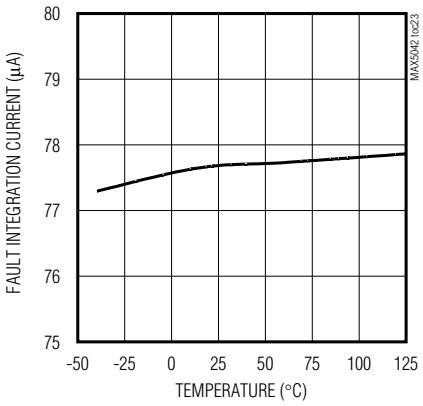
PPWM TO XFRMRL SKEW vs. R_{DRVDEL}



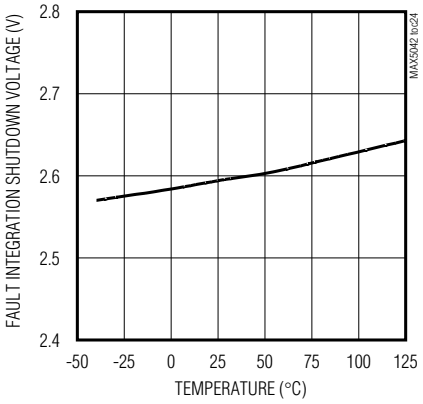
CSA OFFSET vs. TEMPERATURE



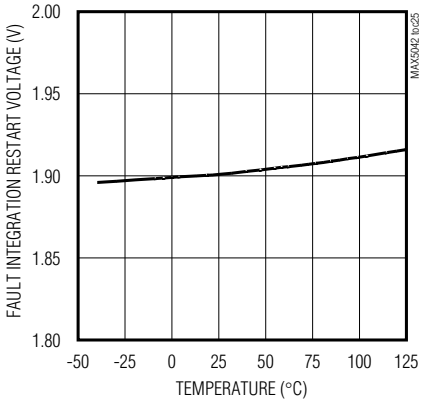
FAULT INTEGRATION CURRENT vs. TEMPERATURE



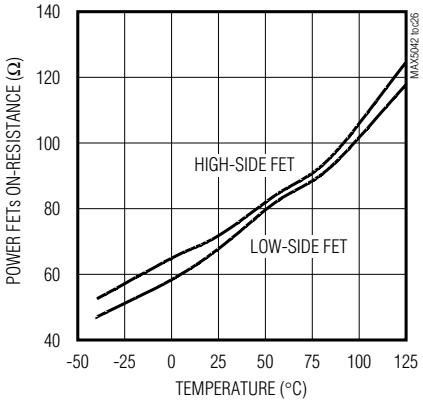
FAULT INTEGRATION SHUTDOWN VOLTAGE vs. TEMPERATURE



FAULT INTEGRATION RESTART VOLTAGE vs. TEMPERATURE



POWER FETs ON-RESISTANCE vs. TEMPERATURE



Two-Switch Power ICs with Integrated Power MOSFETs and Hot-Swap Controller

Pin Description

PIN		NAME	FUNCTION
MAX5042	MAX5043		
1, 2, 14, 15, 40, 42–45, 56	1, 2, 14, 15, 40, 42–45, 56	N.C.	No Connection. Not internally connected.
3	3	RCFF	Voltage-Mode PWM Ramp. Connect a resistor to the input supply and a capacitor to PWMNEG for input voltage feed-forward. Input voltage feed-forward provides instantaneous input-voltage transient rejection and constant loop gain with varying input voltage.
4	4	RAMP	PWM Ramp Input. For voltage-mode control, connect RAMP to RCFF. For current-mode control, connect RAMP to CSOUT, the output of the current-sense amplifier.
5	5	OPTO	Inverting Input of the PWM Comparator. Connect OPTO to the collector of the optotransistor. Connect a pullup resistor from OPTO to REG5.
6	6	CSS	Soft-Start. Connect a capacitor from CSS to PWMNEG to soft-start the converter.
7	7	BST	Boost-Capacitor Bypass for High-Side MOSFET Gate Drive. Connect a 0.1µF capacitor from BST to XFRMRH for the internal high-side MOSFET driver.
8	8	DRVIN	Low-Side MOSFET Driver Supply. Bypass DRVIN with a 0.22µF capacitor to PWMPNEG.
9	9	PWMPNEG	Low-Side MOSFET Driver Return. Connect PWMPNEG externally to PWMNEG with a short trace.
10	10	RCOSC	Oscillator Timing Resistor and Capacitor Connection. Connect a capacitor from RCOSC to PWMNEG and a resistor from RCOSC to REG5. The switching frequency is half the frequency of the sawtooth signal at this connection.
11	11	FLTINT	Fault Integration Input. Use FLTINT in addition to cycle-by-cycle current limit. During persistent current-limit faults, a capacitor connected to FLTINT charges with an internal 80µA current source. Switching terminates when the voltage reaches 2.7V. An external resistor connected in parallel discharges the capacitor. Switching resumes when the voltage drops to 1.8V.
12	12	SYNC	Synchronization Input. The switching frequency of the power supply is half the synchronization frequency, ensuring less than 50% maximum duty cycle.
13	13	$\overline{\text{PWMSD}}$	Latched Shutdown Input. Pull $\overline{\text{PWMSD}}$ low with respect to PWMNEG to stop switching. To restart, release $\overline{\text{PWMSD}}$ and cycle the input supply. Do not leave $\overline{\text{PWMSD}}$ unconnected. Use $\overline{\text{PWMSD}}$ to prevent catastrophic secondary rectifier overheating by monitoring the temperature and issuing a shutdown command with an optocoupler. Connect $\overline{\text{PWMSD}}$ to REG5 when not used.
16, 17, 20, 21, 24	16, 17, 20, 21, 24	SRC	Source Connection for the Internal Low-Side Power MOSFET. Connect SRC to PWMPNEG with a low-value resistor for current limiting.
18, 19, 22, 23	18, 19, 22, 23	XFRMRL	Low-Side Connection for the Isolation Transformer
25	—	POSINHS	Hot-Swap Controller Positive Input Supply (MAX5042 Only). Connect POSINHS along with POSINPWM to the most positive rail of the input supply.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX5042	MAX5043		
26	—	$\overline{\text{HSOK}}$	Hot-Swap OK (MAX5042 Only). $\overline{\text{HSOK}}$'s open-drain output is forced to NEGIN upon hot-swap completion.
27	—	HSEN	Hot-Swap Enable (MAX5042 Only). HSEN is the center point of the internal hot-swap UVLO divider. Use an external voltage-divider or a 100kΩ pullup resistor to the most positive rail to override.
28, 29	—	NEGIN	Negative Supply Input (MAX5042 Only). NEGIN connects to the most negative input supply rail. NEGIN provides the hot-swap circuit's most negative connection. NEGIN is at the same potential as the IC substrate.
30	—	HSGATE	Hot-Swap Gate (MAX5042 Only). Connect HSGATE to the gate of the external hot-swap MOSFET.
31	—	HSDRAIN	Hot-Swap MOSFET Drain Sense (MAX5042 Only). Connect HSDRAIN to the drain of the external hot-swap MOSFET.
32	32	CSOUT	Current-Sense Amplifier Output. The amplifier has a gain of 10. Connect CSOUT to RAMP for current-mode control.
33	33	CSP	Positive Current-Sense Connection. Place the current-sense resistor as close as possible to the device and use a Kelvin connection.
34	34	CSN	Negative Current-Sense Connection. Place the current-sense resistor as close as possible to the device and use a Kelvin connection.
35	26, 28, 29, 31, 35	PWMNEG	Analog Signal Return for the PWM Section
36	36	DRVDEL	Driver Delay Adjust Connection. Connect a resistor and a 0.22µF capacitor from DRVDEL to PWMNEG. The resistor at DRVDEL controls the skew between the PPWM signal and the power pulse applied to the internal power MOSFETs. Use in conjunction with a secondary-side synchronous-rectifier controller. The skew allows for the optimization of the synchronous-rectifier drive pulse.
37	37	PPWM	PWM Pulse Output. PPWM leads the internal power MOSFET pulse by an amount determined with the resistor value at DRVDEL.
38	38	REG9	9V Internal Regulator Output. Use primarily as a source for the internal gate drivers. Bypass REG9 to PWMNEG with a 1µF ceramic capacitor.
39	39	REG5	5V Internal Regulator Output. Bypass REG5 to PWMNEG with a 1µF ceramic capacitor.
41	41	REG15	15V Startup Regulator Output. A voltage greater than 18V on REG15 disables the regulator. Bypass REG15 to PWMNEG with at least one 1µF ceramic capacitor.
46	46	UVLO	PWM Undervoltage Lockout. UVLO is the center point of the PWM undervoltage lockout divider. Use an external divider or a 100kΩ pullup resistor to POSINPWM to override. Connect the external resistor-divider network from POSINPWM to PWMNEG.

Two-Switch Power ICs with Integrated Power MOSFETs and Hot-Swap Controller

Pin Description (continued)

PIN		NAME	FUNCTION
MAX5042	MAX5043		
47	25, 47	POSINPWM	PWM Analog Positive-Supply Input. Connect POSINPWM to the most positive input supply rail.
48, 51, 54, 55	48, 51, 54, 55	DRNH	Drain Connection of the Internal High-Side PWM Power MOSFET. Connect DRNH to the most positive rail of the input supply.
49, 50, 52, 53	49, 50, 52, 53	XFRMRH	High-Side Connection for the Isolation Transformer
—	27	DEN	Delayed Enable Input (MAX5043 Only). DEN is the center point of the delayed enable divider. Use an external voltage-divider or a 100kΩ pullup resistor to the most positive rail to override.
—	30	N.C.	No Connection (MAX5043 Only). Leave unconnected.

Detailed Description

The MAX5042/MAX5043 PWM multimode power ICs are designed for the primary side of voltage or current-mode isolated, forward or flyback power converters. These devices provide a high degree of integration aimed at reducing the cost and PC board area of isolated output power supplies. Use the MAX5042/MAX5043 primarily for 24V, 42V, or 48V power bus applications.

The MAX5042/MAX5043 provide a complete system capable of delivering up to 50W of output power. The MAX5042 contains a hot-swap controller in addition to the PWM and power MOSFETs. The hot-swap section requires an external MOSFET (QHS). Figure 1 details the MAX5042 conceptual block diagram. C_{IN} represents the input bulk storage capacitance of the PWM circuit that requires the soft-start to reduce the inrush current from the backplane. When input power is applied, capacitor C_{IN} is completely discharged and QHS is off. An applied voltage higher than the default undervoltage lockout threshold of the hot-swap controller (30.5V) for more than 165ms (internal turn-on delay) causes the gate voltage of QHS to start gradually increasing. This results in a controlled slew-rate turn-on. The drain voltage of QHS falls at a rate of approximately 10V/ms, drawing a current load from the backplane of approximately 1A for each 100µF of C_{IN} capacitance. The MAX5042's PWM block is prevented from starting up until the QHS MOSFET is fully enhanced. After QHS completely turns on and the voltage across capacitor C_{IN} is above the default startup voltage (31V) of the PWM section, the hot swap enables the PWM block and the soft-start cycle begins. Soft-start limits the amount of current initially drawn from the primary during startup and also prevents possible output-voltage overshoots.

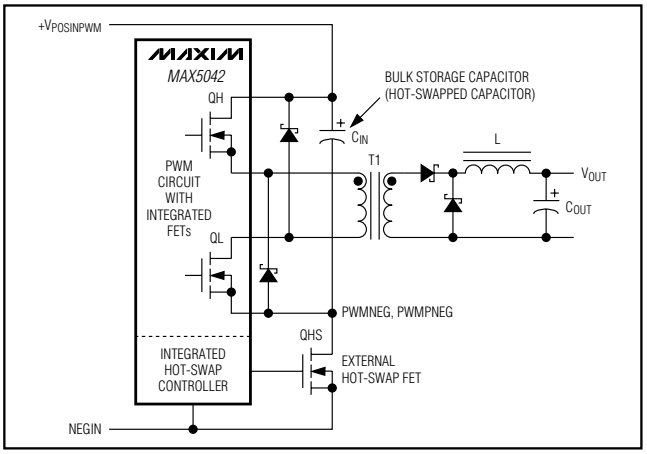


Figure 1. Simplified Diagram of a MAX5042-Based Isolated Power Supply

The MAX5043, detailed in Figure 2, does not contain an integrated hot-swap controller. The MAX5043 begins operating when the input voltage exceeds both of the undervoltage lockout voltages (at UVLO and DEN pins) for 10ms.

The MAX5042/MAX5043 support both forward and flyback power topologies. In forward mode, the maximum output power is approximately 50W. In flyback mode, the maximum output power is approximately 20W. The amount of power dissipated by the package limits the output power. The MAX5042/MAX5043's QFN package features an exposed metal pad on the bottom of the package. Solder the exposed pad directly to the most negative supply in the system. Use a large copper area to improve heat dissipation. Facilitate heat transfer with thermal vias.

Two-Switch Power ICs with Integrated Power MOSFETs and Hot-Swap Controller

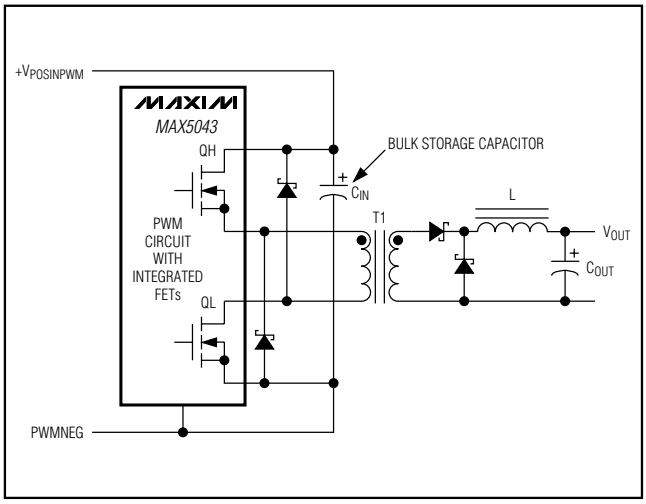


Figure 2. Simplified Diagram of a MAX5043-Based Isolated Power Supply

Set the switching frequency with a resistor and a capacitor at RCOSC. Switching at 250kHz ensures switching losses are minimal and external power passives are small enough for a compact circuit.

The MAX5042/MAX5043 incorporate an advanced set of protection features that make them uniquely suitable when high reliability and comprehensive fault protection are required, as in telecommunication equipment power-supply applications. The MAX5042/MAX5043 15V linear regulator output powers the 9V and 5V regulators used to drive the gates and internal circuitry. A tertiary winding connects to REG15 through a rectifier to power the device after startup and reduces power dissipation in the MAX5042/MAX5043 package. When REG15 is externally powered, the internal 15V regulator is disabled.

Figures 3 and 4 show the block diagrams of the MAX5042 and MAX5043, respectively. The power-OK signals from the hot-swap section, regulators, thermal shutdown, and UVLO combine to generate the internal shutdown signal SHDN. When asserted, SHDN disables the comparators and oscillator. Deasserting SHDN releases the comparators and oscillators. The falling edge of SHDN is delayed allowing the internal signals to settle before the PWM pulses appear. During the time between the falling edge of SHDN and its delayed signal, the 10Ω internal MOSFET (QB) from XFRMRH to PWMPNEG turns on, charging the BST capacitor. After startup, this MOSFET also turns on for approximately 300ns at each half period to help charge the BST capacitor.

Power Topology

The two-switch forward-converter topology offers outstanding robustness against faults and transformer saturation while affording efficient use of the integrated 75mΩ power MOSFETs. Voltage-mode control with feedforward compensation allows the rejection of input supply disturbances within a single cycle similar to that of current-mode controlled topologies. This control method offers some significant benefits when compared with current-mode control. These benefits include:

- No minimum duty-cycle requirement due to current-signal filtering or blanking.
- Clean modulator ramp and higher amplitude for increased stability.
- Stable bias point of the optocoupler LED and phototransistor for maximized control-loop bandwidth (in current-mode applications, the optocoupler bias point is output-load dependent).
- Predictable loop dynamics simplifying the design of the control loop.

The two-switch power topology recovers energy stored in both the magnetizing and parasitic leakage inductances of the transformer. Figure 7 shows the schematic diagram of a 48V input and 5V, 8A output isolated power supply built with the MAX5042.

The MAX5042/MAX5043 also support current-mode control. Current-mode control has advantages such as a single-pole power circuit and a small-signal transfer function that simplify the design of power supplies with widely varying output capacitors.

Undervoltage Lockout

The MAX5042 has two UVLO functions. Both the hot-swap section and the PWM section contain their own undervoltage lockout comparators (HSEN and UVLO, respectively). The MAX5043 lacks the hot-swapping function, but retains the PWM UVLO and the deglitched undervoltage lockout/power-on reset. In both cases, internal resistors set a default input-voltage enable threshold of 31V (typ).

The PWM default input voltage threshold value can be adjusted by using an external divider in parallel with the internal divider. The tolerances of the external divider resistors dominate the precision of the UVLO trip point if their values are smaller than those of the internal divider. Override the default threshold by using:

$$R_{He} = \frac{R_{Le} \times R_{Li} \times R_{Hi} \times (V_{IN} - V_{REF})}{V_{REF} \times R_{Hi} \ (R_{Li} + R_{Le}) - R_{Le} \times R_{Li} \times (V_{IN} - V_{REF})}$$

Two-Switch Power ICs with Integrated Power MOSFETs and Hot-Swap Controller

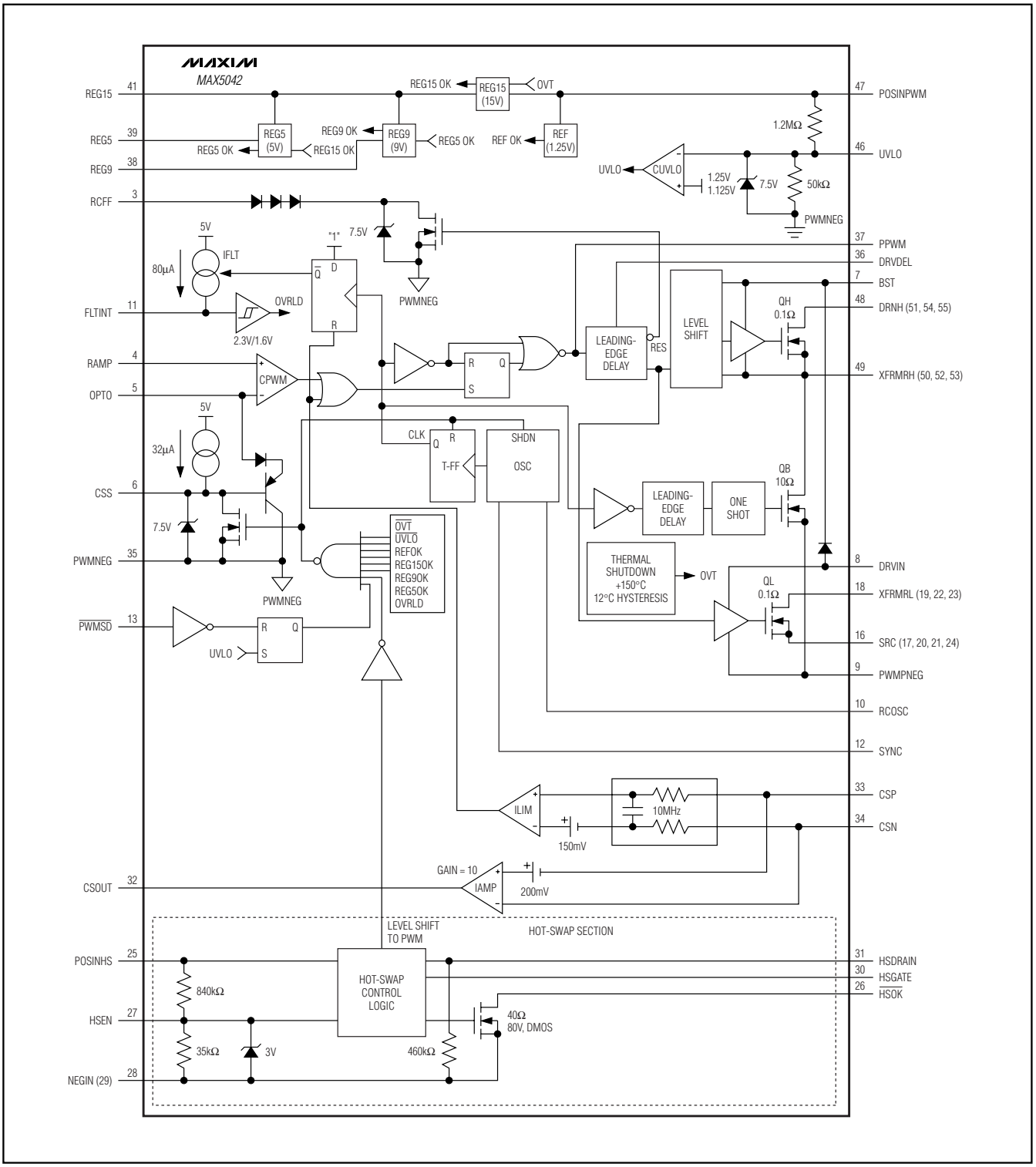


Figure 3. Block Diagram of the MAX5042 Power IC

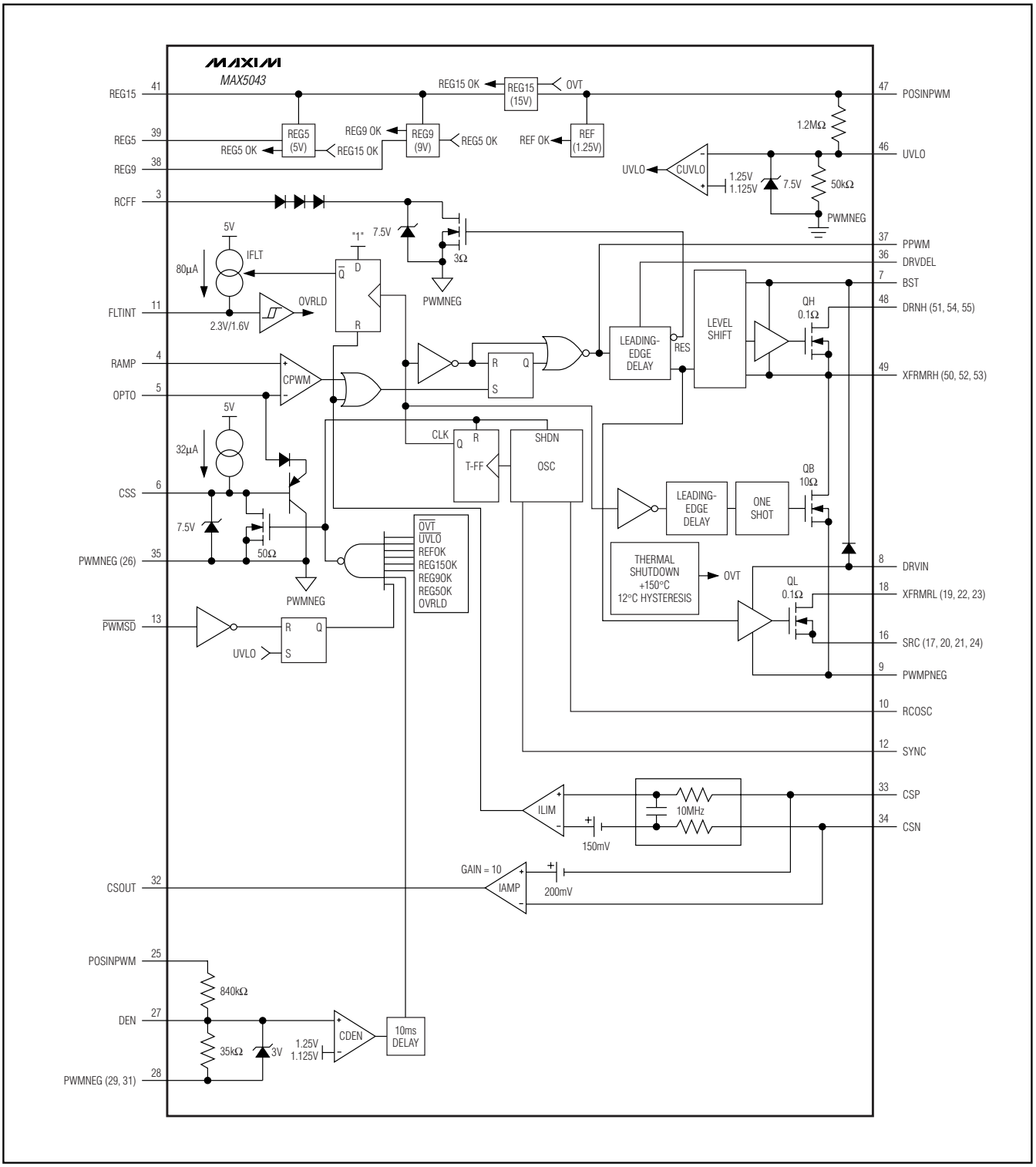


Figure 4. Block Diagram of the MAX5043 Power IC

Two-Switch Power ICs with Integrated Power MOSFETs and Hot-Swap Controller

where R_{HE} is the external high-side resistor, R_{LE} is the external low-side resistor, R_{HI} is the internal high-side resistor (1.2MΩ, typ), R_{LE} is the internal low-side resistor (50kΩ, typ), V_{REF} is 1.27V (typ), and V_{IN} is the desired threshold.

Use an external 100kΩ pullup resistor to POSINPWM to override UVLO functionality for either lockout.

Internal Regulators

An internal high-voltage linear regulator provides a 15V output at REG15. This serves as the input to the 9V regulator that provides bias for the internal MOSFET drivers. The 15V regulator also provides the bias for REG5, a 5V supply used both by internal as well as external circuitry. Bypass the REG15, REG9, and REG5 regulators with 1µF ceramic capacitors. A voltage greater than 18V and less than 40V on REG15 disables the internal high-voltage startup regulator. The REG9 regulator steps down the voltage on REG15 to an output of 9V with a current limit of 100mA. The REG5 regulator steps down the voltage on REG15 to an output of 5V with a current limit of 40mA. Disabling the REG15 regulator by powering REG15 with an external power supply considerably reduces the internal power dissipation in the MAX5042/MAX5043. The voltage and power necessary to override the REG15 internal regulator can be generated with a rectifier and an extra winding from the main transformer.

Soft-Start

Program the MAX5042/MAX5043 soft-start with an external capacitor between CSS and PWMNEG. When the device turns on, the soft-start capacitor (C_{CSS}) charges with a constant current of 33µA, ramping up to 7.3V. During this time, OPTO is clamped to CSS + 0.6V. This initially holds the duty cycle lower than the value the regulator tries to impose, limiting the current inrush and the voltage overshoot at the secondary. When the MAX5042/MAX5043 turn off, the soft-start capacitor internally discharges to PWMNEG.

Secondary-Side Synchronization

The MAX5042/MAX5043 provide convenient synchronization of the secondary-side synchronous rectifiers. Figure 5 shows the connection diagram with a high-speed optocoupler. Choose an optocoupler with a propagation delay of less than 50ns.

For optimum results, adjust the resistor connected to DRVDEL to provide the required amount of delay between the leading edge of the PPWM signal and the turn-on of the power MOSFETs. Use the following formula to calculate the approximate resistance (R_{DRVDEL}) required to set the delay between the PPWM and the power pulse applied to the transformer:

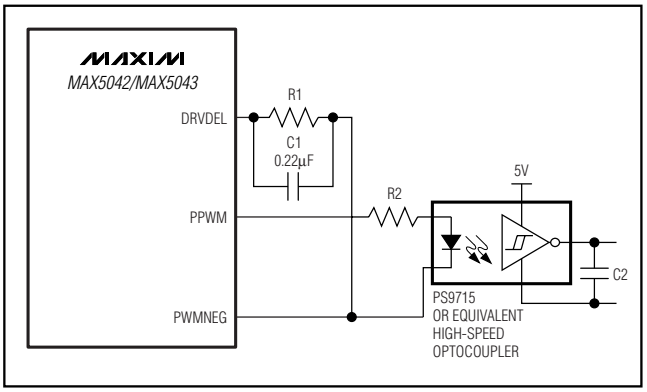


Figure 5. Secondary-Side Synchronous Rectifier Driver Using a High-Speed Optocoupler

$$R_{DRVDEL} = \left(t_{DRVDEL} - (100ns)\right)\left(\frac{k\Omega}{2ns}\right)$$

where t_{DRVDEL} is the required delay from the rising edge of PPWM to the switching of the internal power MOSFETs.

PWM Regulation

The MAX5042/MAX5043 are multimode PWM power ICs supporting both voltage and current-mode control.

Voltage-Mode Control and the PWM Ramp

For voltage-mode control, the feed-forward PWM ramp is generated at RCFF. From RCFF connect a capacitor to PWMNEG and a resistor to POSINPWM. The ramp generated is applied to the noninverting input of the PWM comparator at RAMP and has a minimum voltage of 1.5V to 2.5V. The slope of the ramp is determined by the voltage at POSINPWM and affects the overall loop gain. The ramp peak must remain below the dynamic range of RCFF (0 to 5.5V). Assuming the maximum duty cycle approaches 50% at a minimum input voltage (PWM UVLO turn-on threshold), use the following formula to calculate the minimum value of either the ramp capacitor or resistor:

$$R_{RCFF} \times C_{RCFF} \geq \frac{V_{INUVLO}}{2f_S \times V_{rP\text{-}P}}$$

where:

V_{INUVLO} = the minimum input supply voltage (typically the PWM UVLO turn-on voltage),

f_S = the switching frequency,

$V_{rP\text{-}P}$ = the peak-to-peak ramp voltage (2V, typ).

Maximize the signal-to-noise ratio by setting the ramp peak as high as possible. Calculate the low-frequency, small-signal gain of the power stage (the gain from the inverting input of the PWM comparator to the output) using the following formula:

$$G_{PS} = N_{SP} \times R_{RCFF} \times C_{RCFF} \times f_S$$

where N_{SP} = the secondary to primary power transformer turns ratio.

Current-Sense Amplifier and Current-Mode Control

The MAX5042/MAX5043 can also be programmed for current-mode control (see Figure 6). This control method offers beneficial advantages for certain applications. Current-mode control reduces the order of the output filter, allowing easier control-loop compensation. In current-mode control, the voltage across the current-sense resistor at SRC is amplified by the internal gain-of-10 amplifier IAMP. The cycle-by-cycle current-limit threshold is 156mV. This is the peak voltage amplified by IAMP. A 200mV offset is added to this voltage. The voltage at the output of the current-sense amplifier is:

$$V_{CSOUT} = 2 + 10(V_{CSP} - V_{CSN})$$

The low-frequency, small-signal gain of the power stage (the gain from the inverting input of the PWM comparator to the output) can be calculated using the following formula:

$$G_{PS} = N_{PS} \times \frac{R_L}{R_{SENSE}}$$

where N_{PS} = the primary to secondary power transformer turns ratio,

R_L = the low-frequency output impedance,

R_{SENSE} = the primary current-sense resistor value.

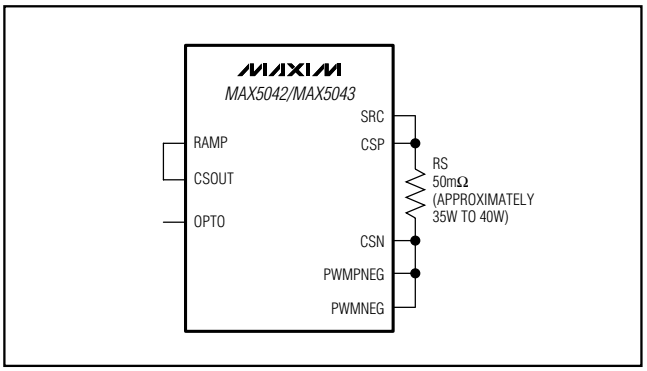


Figure 6. Simplified Connection Diagram for Current-Mode Control

Oscillator and Synchronization

Program the MAX5042/MAX5043 oscillator using an RC network at RCOSC with the resistor connected to REG5 and the capacitor connected to PWMNEG. The PWM frequency is half the frequency at RCOSC.

Use the following formula to calculate the oscillator components:

$$R_{RCOSC} = \frac{1}{2f_S(C_{RCOSC} + C_{PCB})\ln\left(\frac{V_{REG5}}{V_{REG5} - V_{TH}}\right)}$$

where C_{PCB} = 14pF,

REG5 = 5V,

f_S = switching frequency,

V_{TH} = RCOSC peak trip level.

The delay programmed by the resistor at DRVDEL limits the power MOSFET's maximum duty cycle to less than 50 percent.

SYNC allows synchronization of the MAX5042/MAX5043 to an external clock. For proper synchronization, set the external SYNC frequency 15% to 20% higher than the programmed free-running frequency of the MAX5042/MAX5043's internal oscillator. The actual switching frequency will be half the synchronizing frequency.

Integrating Fault Protection

The integrating fault protection feature allows the MAX5042/MAX5043 to ignore transient overcurrent conditions for a programmable amount of time, giving the power supply time to behave like a current source to the load. This can happen, for example, under load-current transients when the control loop requests maximum current to keep the output voltage from going out of regulation. Program the ignore time externally by connecting a capacitor to FLTINT. Under sustained overcurrent faults, the voltage across this capacitor ramps up toward the FLTINT shutdown threshold (typically 2.7V). When FLTINT reaches the threshold, the power supply shuts down. A high-value bleed resistor connected in parallel with the FLTINT capacitor allows the capacitor to discharge toward the restart threshold (typically 1.8V). Crossing the restart threshold soft-starts the supply again.

The ILIM comparator provides cycle-by-cycle current limiting with a typical threshold of 156mV. The fault integration circuit works by forcing an 80µA current out of FLTINT for one clock cycle every time the current-limit comparator (Figures 3 and 4, ILIM) trips. Use the following formula to calculate the approximate capacitance (C_{FLTINT}) needed for the desired shutdown time.

Two-Switch Power ICs with Integrated Power MOSFETs and Hot-Swap Controller

$$C_{FLTINT} \cong \frac{I_{FLTINT} \times t_{SH}}{1.4}$$

where I_{FLTINT} = 80µA,

t_{sh} is the desired ignore time during which current-limit events from the current-limit comparator are ignored.

Some testing may be required to fine tune the actual value of the capacitor.

Calculate the approximate bleed resistance (R_{FLTINT}) needed for the desired recovery time using the following formula:

$$R_{FLTINT} \cong \frac{t_{RT}}{C_{FLTINT} \ln\left(\frac{2.3}{1.6}\right)}$$

where t_{RT} is the desired recovery time.

Choose at least t_{RT} = 10 x t_{SH}. Typical values for t_{SH} range from a few hundred microseconds to a few milliseconds.

Shutdown Modes

Latched Shutdown

The MAX5042/MAX5043 feature a latched shutdown that terminates switching in the event of a serious fault. External faults in synchronously rectified power supplies cause a loss of control for the rectifiers. Either the body or the external Schottky diodes conduct, resulting in a very high power dissipation and a quick rise of the power-supply temperature. A thermal sensor placed on the same ground plane as the secondary-side rectifiers can sense this catastrophic increase in temperature and issue a shutdown signal to $\overline{PWMSD}$. Asserting $\overline{PWMSD}$ stops switching and latches the fault until the power is cycled. Connect $\overline{PWMSD}$ to REG5 to disable latched shutdown.

Functional Shutdown

Shut down the MAX5042/MAX5043 by pulling UVLO to PWMNEG using an open-collector or open-drain transistor connected to PWMNEG. Pulling HSEN to NEGIN also shuts down the MAX5042 after a 10ms turn-off delay. Pulling DEN low also shuts down the MAX5043 with a 1ms turn-off delay. When HSEN is used, the MAX5042 goes through a full hot-swap startup sequence with a 165ms startup delay. The MAX5043 also has a 10ms delay from when DEN asserts.

Thermal Shutdown

The MAX5042/MAX5043 feature internal thermal shutdown. Internal sensors monitor the high-power areas. Thermal faults arise from excessive dissipation in the power FETs or in the regulators. When the temperature limit is reached, switching is terminated and the regulator shuts down. The integration of thermal shutdown and the power MOSFETs result in a very robust power circuit.

MAX5042 Hot-Swap Controller

The MAX5042 integrates a PWM power IC with a hot-swap controller. The design allows a power supply built around the MAX5042 to be safely hot-plugged into a live backplane without causing a glitch on the power-supply rail. The hot-swap section operates from POSINHS to NEGIN. The MAX5042 only requires an external N-channel MOSFET to provide hot-swap control. Figures 1 and 3 detail hot-swap functionality.

The MAX5042 controls an external N-channel power MOSFET placed in the negative power-supply pathway. When power is applied, the MAX5042 keeps the MOSFET off. The MOSFET remains off indefinitely if HSEN is below 1.26V, POSINHS is below the undervoltage lockout level (31V), or the die temperature exceeds +150°C. If none of these conditions exist for 165ms, the MAX5042 gradually turns on the MOSFET, allowing the voltage on HSDRAIN to fall no faster than 10V/ms. During this period, the PWM block remains in shutdown. The inrush current through the external MOSFET (and therefore through the capacitor C_{IN}) is limited to a level proportional to its capacitance, and the constant HSDRAIN slew rate. After the MOSFET completely turns on, and HSDRAIN falls to its final value, the hot-swap period is terminated and the PWM section of the IC powers up.

HSEN offers external control of the MAX5042, facilitating power-supply sequencing. HSEN can also be used to change the undervoltage lockout level using an external divider network, if necessary. Undervoltage lockout keeps the external hot-swap MOSFET switched off as long as the magnitude of the input voltage is below the desired level. There is a 10ms turn-off delay on the HSEN signal.

A power-good output, $\overline{HSOK}$, asserts when the external MOSFET completely turns on. $\overline{HSOK}$ is an open-drain output referenced to NEGIN, and can withstand up to 80V above NEGIN.

Determining Hot-Swap Inrush Current

Calculate the hot-swap inrush current using the following formula:

$$I_{C_{IN}} = C_{IN}\frac{dV_{HSDRAIN}}{dt} = C_{IN}S_{HSLR}$$

where:

C_{IN} = the load capacitance,

S_{HSLR} is the MAX5042 hot-swap slew rate magnitude given in the *Electrical Characteristics* table.

For example, assuming an input bulk capacitance of 100µF, and using the typical value of 10V/ms for the slew rate, the calculated inrush current is 1A. See Table 1 for suggested external hot-swap MOSFETs.

Table 1. MAX5042 Suggested External Hot-Swap MOSFETs

MAXIMUM I_{LOAD} (A)	SUGGESTED EXTERNAL MOSFET
0.25	IRFL110
0.5	IRFL4310
1	IRFR3910
2	IRF540NS
3	IRF1310NS
4	IRF1310NS

Typical Application Circuits

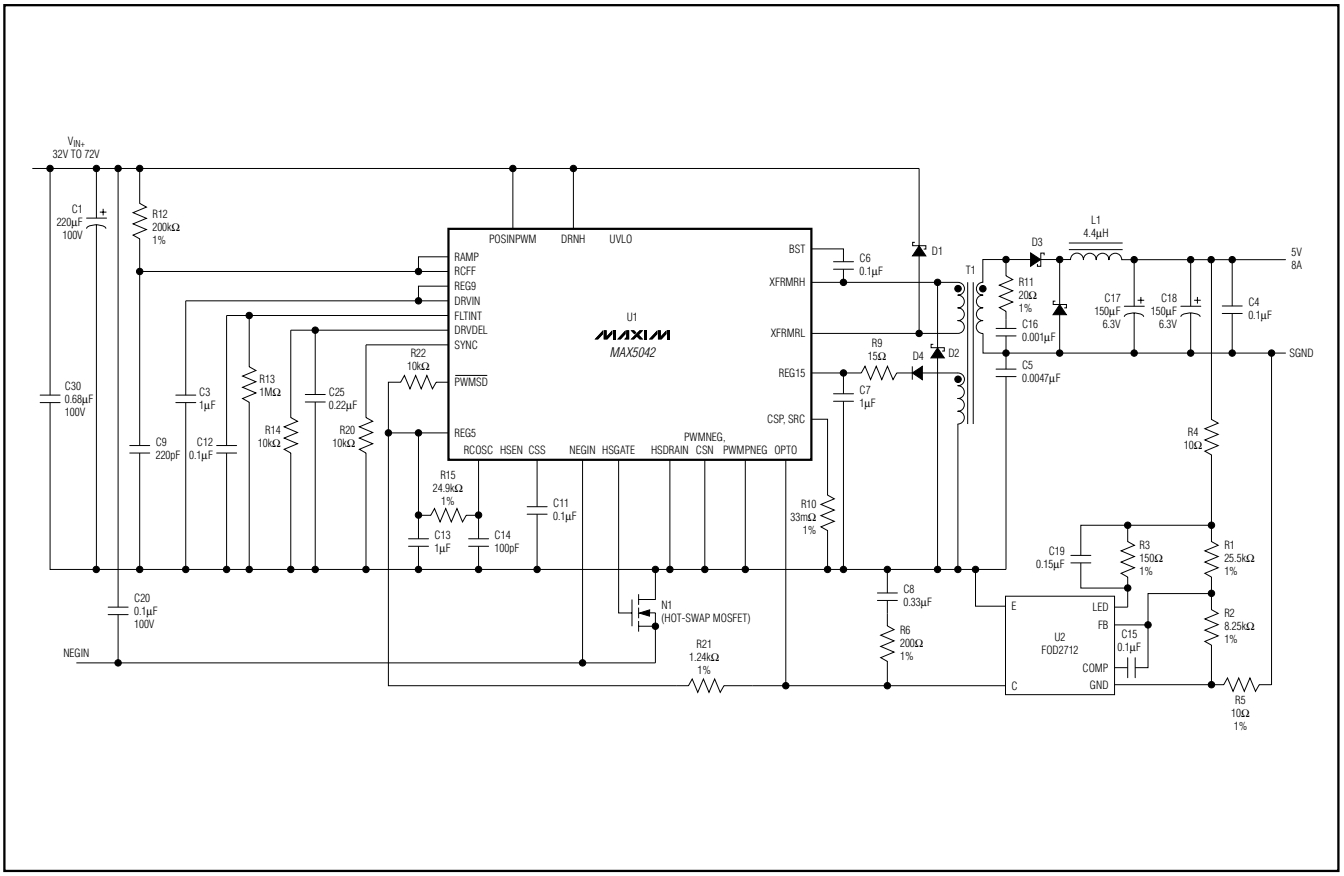


Figure 7. MAX5042 Typical Application Circuit (48V Power Supply with Hot-Swap Capability)

Two-Switch Power ICs with Integrated Power MOSFETs and Hot-Swap Controller

Typical Application Circuits (continued)

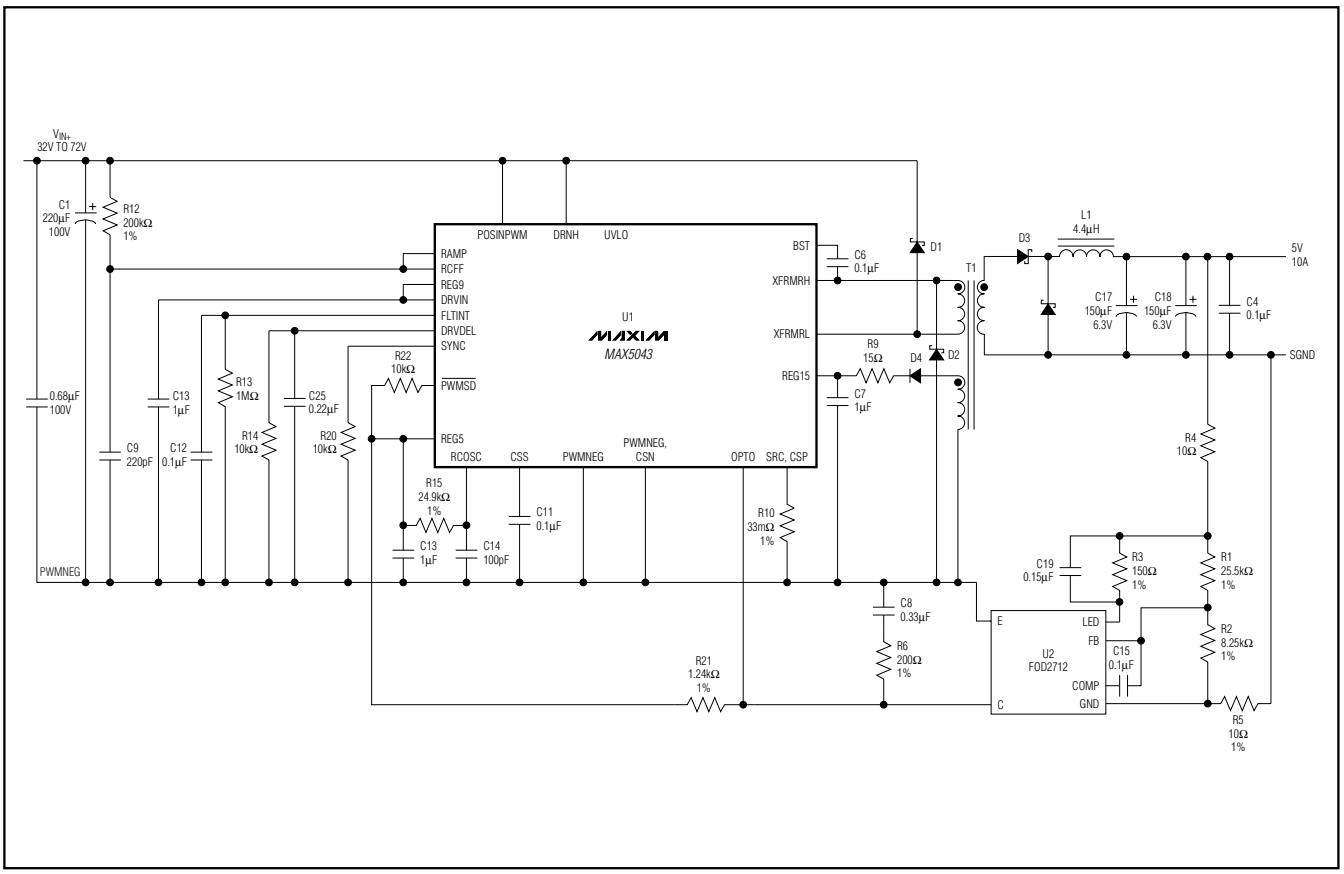
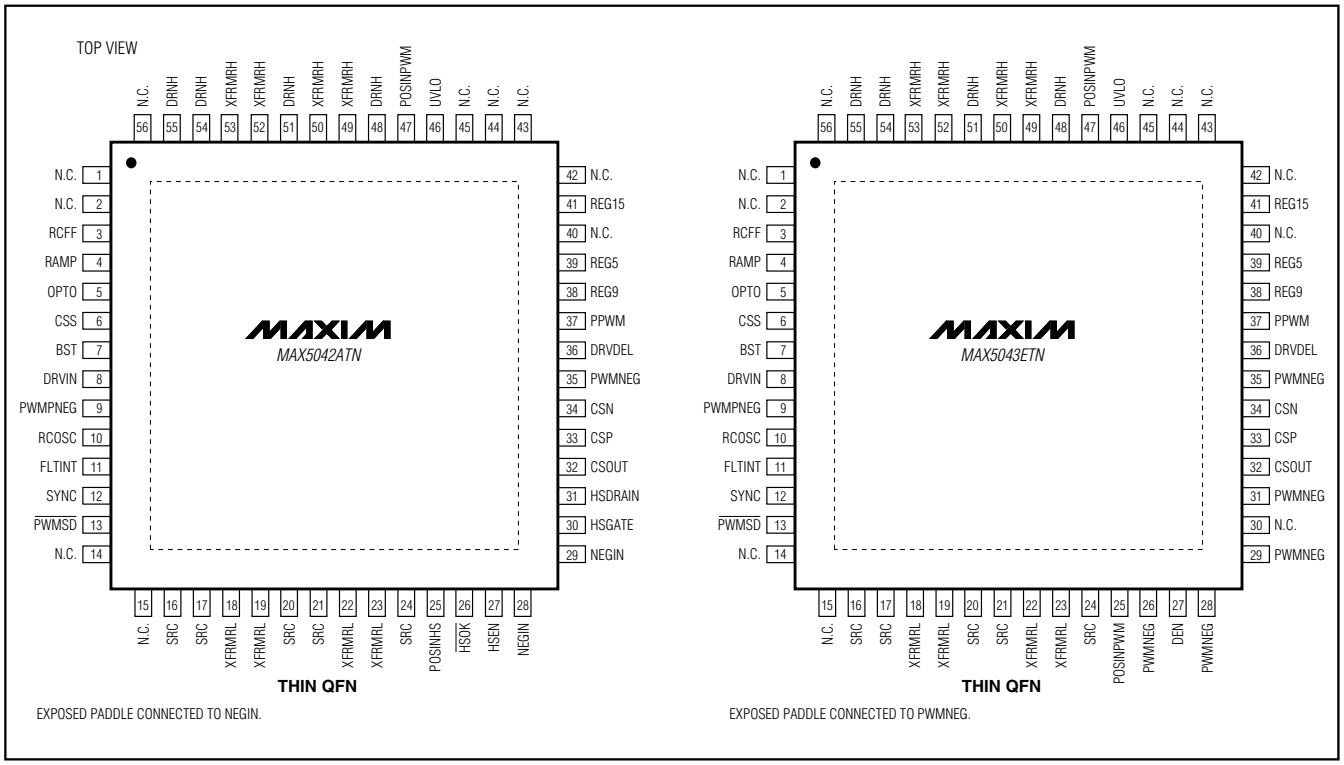


Figure 8. MAX5043 Typical Application Circuit (48V Power Supply without Hot-Swap Capability, this Circuit has not been Tested)

Two-Switch Power ICs with Integrated Power MOSFETs and Hot-Swap Controller

Pin Configurations



Chip Information

TRANSISTOR COUNT: 35,247

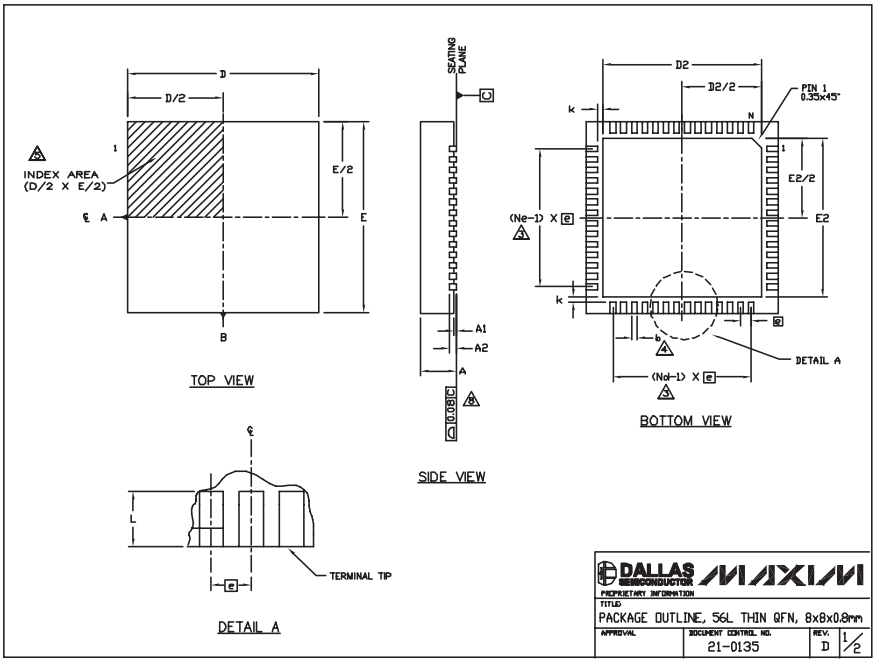
PROCESS: BiCMOS DMOS

Two-Switch Power ICs with Integrated Power MOSFETs and Hot-Swap Controller

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

56L THIN QFN.EPS



DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 56L THIN QFN, 8x8x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0135	D	1/2

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.225mm MAXIMUM (0.009 INCHES MAXIMUM).
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE LOCATED ON THE TOP SURFACE OF THE PACKAGE WITHIN HATCHED AREA AS SHOWN.
   EITHER AN INDENTATION MARK OR INK/LASER MARK IS ACCEPTABLE.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. PACKAGE WARPAGE MAX 0.01mm.
8. APPLIES TO EXPOSED PAD AND TERMINALS.
   EXCLUDES INTERNAL DIMENSION OF EXPOSED PAD.
9. MEETS JEDEC MO220.

SYMBOL	56L 8x8			NOTE
	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	
b	0.20	0.25	0.30	4
D	7.90	8.00	8.10	
E	7.90	8.00	8.10	
e	0.50 BSC			
N	56			3
Nd	14			3
Ne	14			3
L	0.30	0.40	0.50	
A1	0.00	0.02	0.05	
A2	0.20 REF			
k	0.25	--	--	

PKG. CODE	EXPOSED PAD VARIATION						JEDEC	DOWN BONDS ALLOWED
	D2			E2				
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
T5688-1	6.50	6.65	6.70	6.50	6.65	6.70	WLLD-5	NO
T5688-2	6.50	6.65	6.70	6.50	6.65	6.70	WLLD-5	YES
T5688-3	6.50	6.65	6.70	6.50	6.65	6.70	WLLD-5	NO

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 56L THIN QFN, 8x8x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0135	D	2/2